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(54) **ACTIVE MATRIX DISPLAY DEVICE**

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G09G 5/10	(2006.01)

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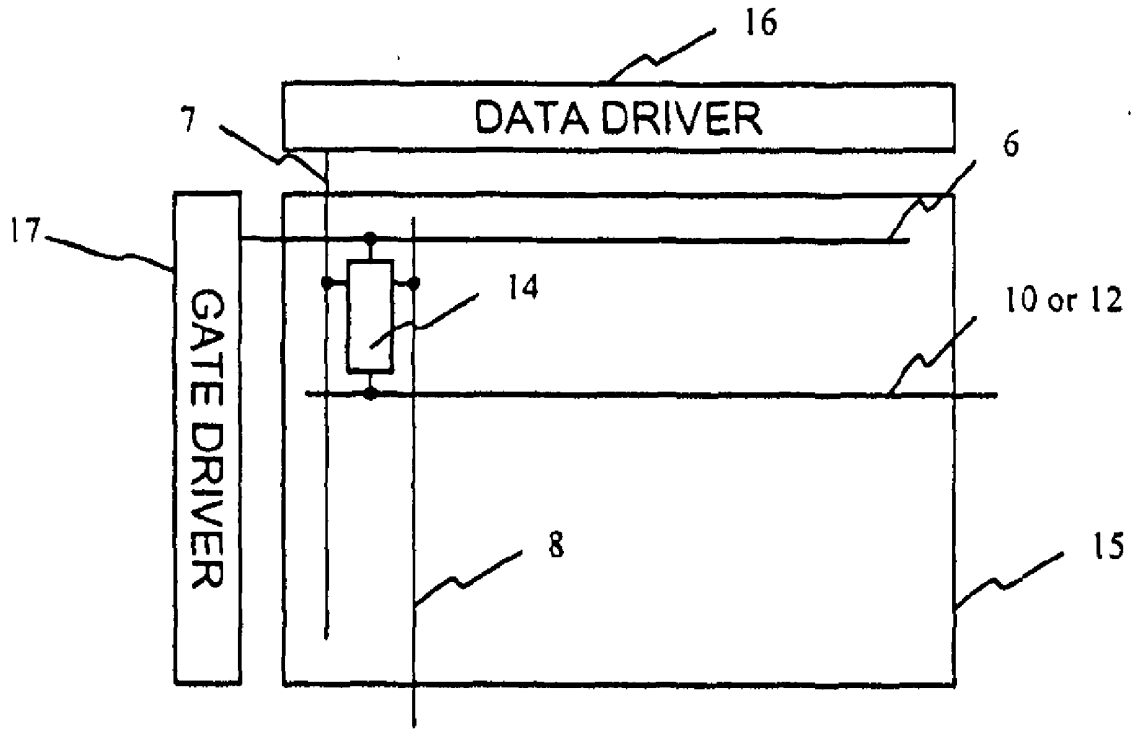
(57) **ABSTRACT**

The application aims at reducing the power consumption of pixels not emitting light in an active matrix organic EL panel having a static memory cell in each pixel. Each pixel circuit comprises a selection transistor (**5**), first (**2**) and second (**4**) drive transistors as well as a first organic EL element (**1**) and a second (**3**) organic EL element respectively connected to the first and second drive transistors. The second organic. EL element is masked and does not contribute to the pixel brightness. The current flowing through the second organic EL element is reduced by current limiting means. This current limiting means may be a second supply voltage (VDD**2**) used in the current path with the second organic EL element, the second supply voltage being lower than the corresponding first supply voltage (VDD**1**) of the current path with the first organic EL element. Alternatively, the current limiting means may comprise a current limiting transistor (**11**) or a diode-connected transistor (**13**).



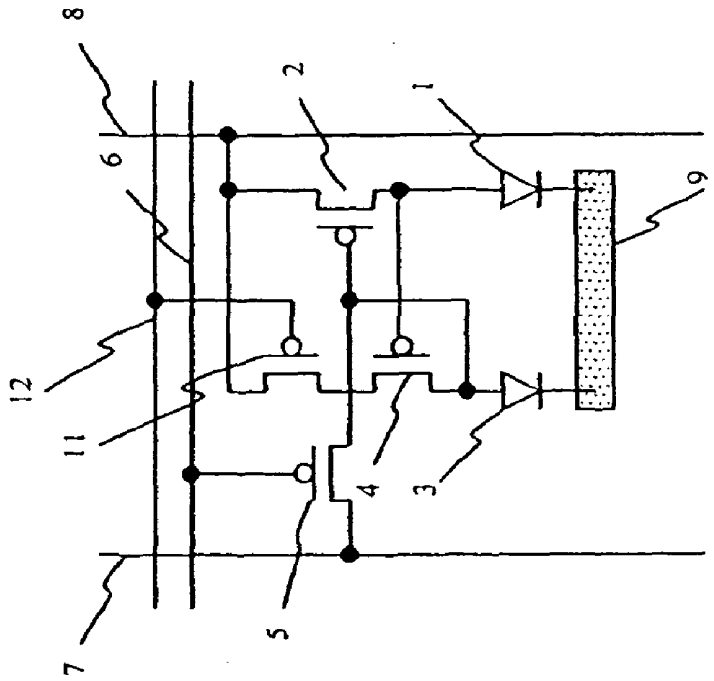


Fig. 2

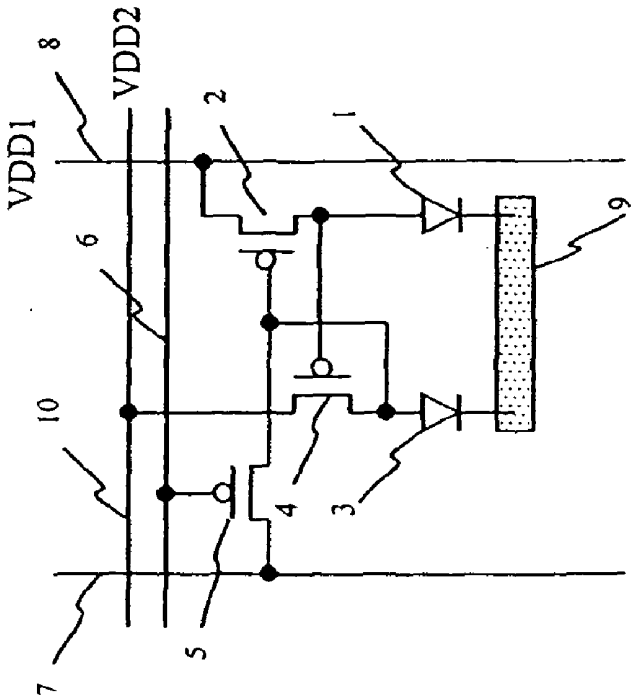


Fig. 1

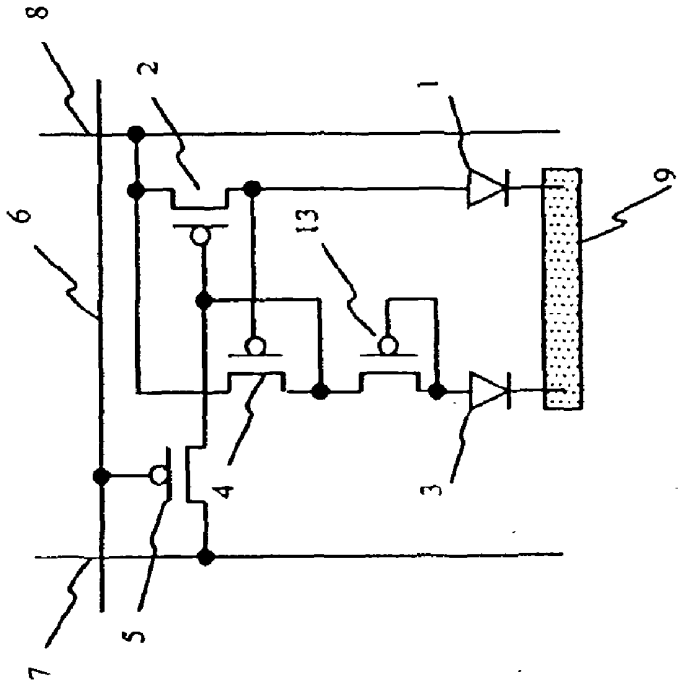


Fig. 4

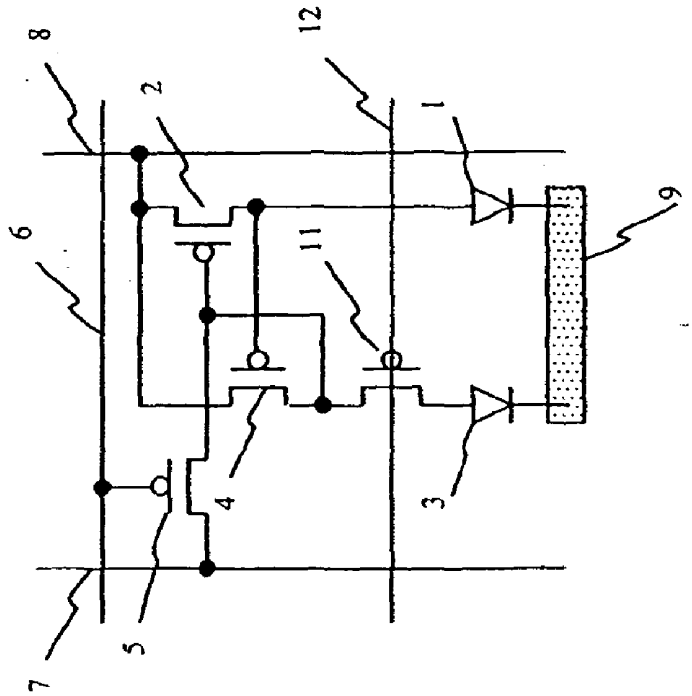


Fig. 3

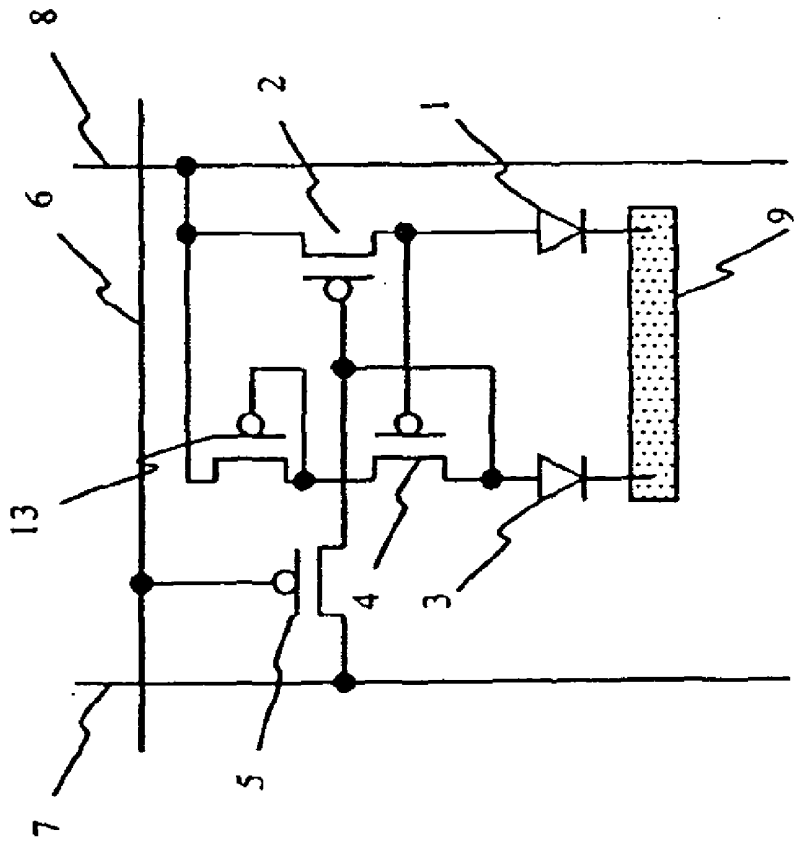


Fig. 5

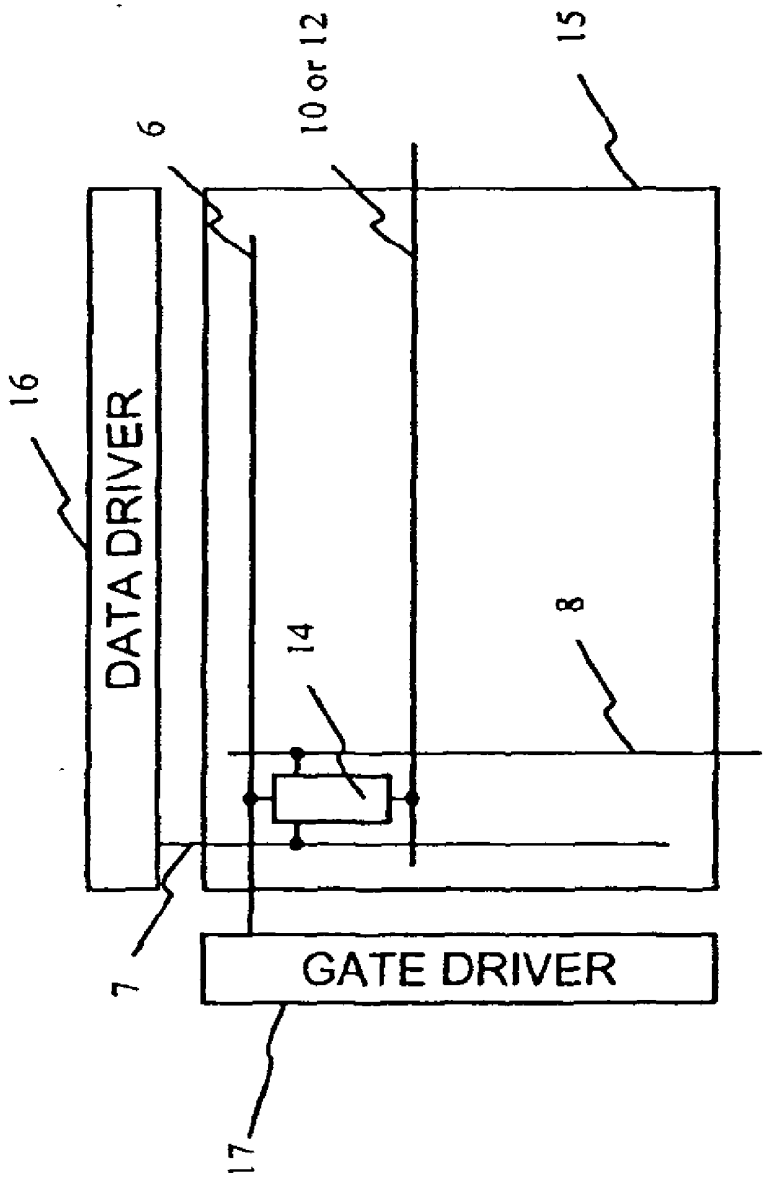


Fig. 6

ACTIVE MATRIX DISPLAY DEVICE

FIELD OF THE INVENTION

[0001] The present invention relates to an active matrix display device comprising, in each pixel arranged in a matrix form, a self-emitting element and an element which controls light emission of the self-emitting element.

BACKGROUND OF THE INVENTION

[0002] Active matrix display devices are capable of being made high resolution, and so are becoming widespread as displays. Active matrix display devices currently require active elements in order to determine a display state one pixel at a time. Particularly in the case of a current drive device such as an organic EL display, drive transistors capable of supplying electrical current to the light-emitting elements are provided. A thin film transistor (TFT) formed from a thin film such as amorphous silicon or polysilicon is used as such a drive transistor, but it is difficult to achieve uniform characteristics in a TFT.

[0003] A number of methods have been proposed for correcting TFT characteristics using circuit technology, one of which is digital drive, which is a known method for controlling gradation using digital drive of an active matrix organic EL display. For example in WO 2005/116971.

[0004] However, with digital drive 1 frame period is divided into a plurality of sub-frame periods, and bit data is written to control whether or not light is emitted in each sub-frame period. It is therefore necessary to write bit data for a pixel in 1 frame period by a number of times that is the same as the number of sub-frames.

[0005] In this way, in the case of digital drive to write digital data corresponding to respective bit data divided into sub-frames many times in a single frame period, if the wiring capacitance of the panel is large the power consumption will tend to be large. In particular, even if there is no image variation if the panel size is increased, power is consumed in order to write the bit data.

SUMMARY OF THE INVENTION

[0006] The present invention is directed to an active matrix display device comprising, in each of a plurality of pixels arranged in a matrix form, a self-emitting element and an element which controls light emission of the self-emitting element, wherein each pixel includes, a static memory in which a first transistor of a pair of transistors is switched ON or OFF according to a supplied signal and a second transistor of the pair of transistors is switched OFF or ON according to an output voltage of the first transistor, so that the static memory maintains a state according to the supplied signal, and a pair of self-emitting elements each connected to each of the pair of the transistors of the static memory wherein a first self-emitting element contributes to display when a current is supplied and a second self-emitting element does not contribute to display even when a current is supplied, and wherein a current flowing through the second self-emitting element which does not contribute to display is reduced within a range which does not affect the state maintenance by the static memory.

[0007] Also, a power supply voltage for supplying current to the transistor, of the pair of transistors of the static memory, that is connected to the self-emitting element that does not contribute to display, is preferably made a lower voltage compared to the power supply for supplying current to the other transistor.

[0008] It is also possible for the transistors of the static memory to have a separate current control transistor connected in series with the transistor connected to the self-emitting element that does not contribute to display, and to adjust current amount flowing in the self-emitting element that does not contribute to display by adjusting the current amount of this current control transistor.

[0009] It is also possible for the transistors of the static memory to have a separate diode connected current control transistor connected in series with the transistor connected to the self-emitting element that does not contribute to display, and to reduce current amount flowing in the self-emitting element that does not contribute to display. It is also possible for the self-emitting element to be an organic EL element.

[0010] According to the present invention, by reducing a current flowing through a self-emitting element which does not contribute to display within a range which does not affect the state maintenance by the static memory, it is possible to lower the current amount when pixels are not emitting light.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** is a drawing showing a pixel circuit for limiting current using a second power supply voltage;

[0012] FIG. **2** is a drawing showing a pixel circuit for limiting current using a current limiting transistor;

[0013] FIG. **3** is a drawing showing another pixel circuit for limiting current using a current limiting transistor;

[0014] FIG. **4** is a drawing showing a pixel circuit for limiting current using a diode transistor;

[0015] FIG. **5** is a drawing showing another pixel circuit for limiting current using a current diode transistor; and

[0016] FIG. **6** is a drawing showing the overall structure of a display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Embodiments of the present invention will be described in detail in the following using the drawings.

[0018] A pixel circuit of the present invention is shown in FIG. **1**. The pixel circuit shown in FIG. **1** includes a first organic EL element **1** that contributes to display, a first drive transistor **2** for controlling lighting of the first organic EL element **1**, a second organic EL element **3** that does not contribute to display, a second drive transistor **4** that controls lighting of the second organic EL element **3**, and a gate transistor **5** that conveys data from a data line **7** to a gate terminal of the first drive transistor **2** in accordance with a selection signal supplied to a gate line **6**.

[0019] An anode of the first organic EL element **1** is connected to a drain terminal of the first drive transistor **2** and the gate terminal of the second drive transistor **4**. An anode of the second organic EL element **3** is connected to the drain terminal of the second drive transistor **4**, the gate terminal of the first drive transistor **2**, and the source terminal of the gate transistor **5**. The gate terminal of the gate transistor **5** is connected to the gate line **6**, while the drain terminal of the gate transistor **5** is connected to the data line **7**. A source terminal of the first drive transistor **2** is connected to a first power supply line **8** for supplying a first power supply voltage VDD**1**, a source terminal of the second drive transistor **4** is

connected to a second power supply line **10** for supplying a second power supply voltage VDD**2**, and cathodes of the first organic EL element **1** and the second organic EL element **3** are connected to a cathode electrode **9** to which a cathode power supply VSS is supplied.

[0020] With this type of structure, if the gate line **6** is selected (Low), digital data (High or Low data) that has been supplied to the data line **7** is conveyed to the gate terminal of the first drive transistor **2**. If the digital data is low, the first drive transistor **2** is turned on, and at the same time as the anode of the first organic EL element **1** and the first power supply line **8** are connected to cause current to flow through the first organic EL element **1**, the gate terminal of the second drive transistor **4** is connected to the first power supply line **8**. Specifically, the second drive transistor **4** is turned off as a result of its gate potential becoming the first power supply potential VDD**1**, and simultaneously with the anode potential of the second organic EL element **3** dropping to the cathode potential VSS the gate of the first drive transistor **2** is also similarly lowered to the cathode potential VSS. As a result, the gate line **6** is made non-selected (High), and even if the gate transistor **5** is off lighting of the first organic EL element **1** continues, and the second organic EL element **3** is kept in an unlit state.

[0021] When the digital data is High, the first drive transistor **2** is turned off, and the anode of the first organic EL element **1** is lowered to the cathode potential VSS, but simultaneously with this the gate potential of the second drive transistor **4** also similarly falls to the cathode potential VSS and the second drive transistor **4** is turned on. If the second drive transistor **4** is turned on, the anode of the second organic EL element **3** is connected to the second power supply line **10**, current is made to flow in the second organic element **3** by the anode of the second organic EL element **3** becoming the second power supply potential VDD**2**, and at the same time the gate potential of the first drive transistor **2** also becomes the second power supply potential VDD**2**. As long as the second power supply potential VDD**2** is a sufficient potential to turn off the first drive transistor **2**, then even if the gate transistor **5** is turned off the first organic EL element **1** is kept unlit and a state where current continues to flow in the second organic EL element **3** is maintained.

[0022] Since the structure is such that the first organic EL element **1** contributes to display by generating light, that is emitted when current flows, to the outside, but the second organic EL element **3** does not contribute to display because emitted light is not released to the outside even if current flows, the operation of the first organic EL element **1** determines a light emitting state of the pixel.

[0023] As a method of giving a structure such that emitted light is not released to the outside, as with the second organic EL element **3**, there is a method of making the second organic EL element **3** itself an element that does not emit light, but this requires manufacturing steps to fabricate the first organic EL element **1** that emits light and the second organic EL element **3** that does not emit light, which complicates the manufacturing process. It is therefore easier to darken the second organic EL element **3** using metal or black matrix etc. so that there is no release of light to the outside. In any case, since the second organic EL element **3** does not contribute to display, formation is preferred where the light emitting surface area of the second organic EL element **3** is made small, and the light emitting surface area of the first organic EL element **1** is made large.

[0024] However, even when constructing the organic EL elements as described above, there is a limit to how small the second organic EL element **3** can be made, and current flowing from the second power supply line **10** is of an extent to maintain the gate potential of the first drive transistor **2** at an off level, even after the gate transistor **5** has been turned off.

[0025] Accordingly, with this embodiment, the second power supply potential VDD**2** supplied to the second power supply line **10** is made smaller than the first power supply potential VDD**1** supplied to the first power supply line **8**, and current flowing in the second organic EL element **3** is limited by setting to a potential sufficient to turn off the first drive transistor **2**, in other words, to at least the threshold voltage of the first drive transistor **2**.

[0026] A potential that makes the power consumption extremely small while maintaining a state where the first organic EL element **1** is not lit is found by appropriately varying the second power supply potential VDD**2**, and if this potential is set as VDD**2**, it is possible to guarantee operation of the static memory while realizing low power consumption.

[0027] A pixel circuit of another embodiment is shown in FIG. **2**. In FIG. **2**, a current limiting transistor **11** is arranged in series between the second drive transistor **4** and the first power supply line **8**. The gate terminal of the current limiting transistor **11** is connected to the current limit line **12**, the source terminal is connected to the first power supply line **8**, and the drain terminal is connected to the source terminal of the second drive transistor **4**.

[0028] A control voltage supplied to the current limit line **12** is required to be at the threshold or below of the current limiting transistor **11** in order for current to flow in the second organic EL element **3**, but it should be a value such that the potential of the second organic EL element **3** at this current is a sufficiently high level to turn the first drive transistor **2** off. That is, a minimum current that allows the second organic EL element **3** to keep the first drive transistor **2** off. In other words, the minimum current can generate a voltage that is the threshold or higher of the first drive transistor **2** so that the first transistor **2** keeps off state, and the first organic EL element **1** can maintain the unlit state by supplying a control voltage generated by the current limiting transistor **11** to the current limit line **12**.

[0029] With FIG. **1**, the structure is such that the off level of the first drive transistor **2** is directly controlled by using the second power supply potential VDD, but with FIG. **2**, by controlling current flowing in the second organic EL element **3** using the current limiting transistor **11** the second power supply voltage VDD**2** is generated and the off level of the first drive transistor **2** is controlled indirectly.

[0030] It is also possible to have the current limiting transistor **11** arranged in series between the second organic EL element **3** and the second drive transistor **4**, with the gate terminal of the current limiting transistor **11** connected to the current limit line **12**, the drain terminal connected to the anode of the second organic EL element **3**, and the source terminal connect to the drain terminal of the second drive transistor **4**, the gate terminal of the first drive transistor **2**, and the source terminal of the gate transistor **5**.

[0031] In this case, by using the current limiting transistor **11** the off voltage generated at the gate terminal of the first drive transistor **2** can be made substantially equal to the first power supply potential VDD **1**, and it is possible to limit the

current flowing in the second organic EL element **3** while maintaining an off state of the first drive transistor **2** in a more stable manner.

[0032] Also, as shown in FIG. **4**, it is possible to arrange a diode transistor, having the gate terminal and drain terminal short circuited and operating as a diode, between the second organic EL element **3** and the second drive transistor **4**, with the drain terminal (gate terminal) connected to the anode of the second organic EL element **3**, and the source terminal connect to the drain terminal of the second drive transistor **4**, the gate terminal of the first drive transistor **2**, and the source terminal of the gate transistor **5**.

[0033] Since the diode transistor **13** and the second organic EL element **3** are connected in series, a larger forward bias voltage is needed and current is limited.

[0034] As shown in FIG. **5**, it is also possible to have the diode transistor **13** arranged between the first power supply line **8** and the second drive transistor **4**, with the source terminal connected to the power supply line **8**, and the drain terminal (gate terminal) connected to the source terminal of the second drive transistor **4**. In this case, the drain side voltage of the diode transistor **13** becomes a voltage supplied to the drain terminal (gate terminal) of the first drive transistor **2** when the second drive transistor **4** is on, namely, a voltage corresponding to the second power supply potential VDD**2** in FIG. **1**. Therefore, the voltage of the drain terminal (gate terminal) of this diode transistor **13** is required to be designed giving sufficient consideration to variations in characteristics of the diode transistor **13**, so that it is made a sufficiently high potential to turn off the first drive transistor **2**.

[0035] FIG. **6** shows a display device includes a pixel array **15** having the pixels **14** of FIG. **1** to FIG. **5** arranged in a matrix array, a gate driver **17** for driving gate lines **6**, and a data driver **16** for driving data lines **7**.

[0036] When a pixel **14** is as shown in FIG. **1**, the second power supply voltage VDD**2** is supplied to the second power supply line **10**, while when configured as shown in FIG. **2** or FIG. **3** the current limit voltage is supplied to the current limit line **12**. With the pixel **14** shown in FIG. **4** or FIG. **5**, the second power supply line **10** and the current limit line **12** are not required, and so they are omitted.

[0037] In this manner, by controlling the voltage and current supplied to the second organic EL element **3** either directly or indirectly using a transistor, it is possible to lower the power consumption when maintaining an unlit state of the first organic EL element **1**.

PARTS LIST

[0038] **1** organic EL element
[0039] **2** first drive transistor
[0040] **3** organic EL element
[0041] **4** second drive transistor
[0042] **5** gate transistor
[0043] **6** gate line
[0044] **7** data line
[0045] **8** first power supply line
[0046] **9** cathode electrode
[0047] **10** second power supply line
[0048] **11** current limiting transistor
[0049] **12** current limit line
[0050] **13** diode transistor
[0051] **14** pixels
[0052] **15** pixel array
[0053] **16** data driver
[0054] **17** gate driver

1. An active matrix display device comprising, in each pixel arranged in a matrix form, a self-emitting element and an element that controls light emission of the self-emitting element, wherein each pixel comprises:

a static memory in which a first transistor of a pair of transistors is switched ON or OFF according to a supplied signal and a second transistor of the pair of the transistors is switched OFF or ON according to an output voltage of the first transistor, so that the static memory maintains a state according to the supplied signal;

a pair of self-emitting elements, each connected to each of the pair of transistors of the static memory, wherein a first self-emitting element contributes to display when a current is supplied and a second self-emitting element does not contribute to display even when a current is supplied; and

means for flowing current through the second self-emitting element which does not contribute to display that is reduced to be within a range which does not affect the state maintenance by the static memory.

2. The active matrix display device of claim **1**, wherein:

a power supply voltage for supplying current to the transistor, of the pair of transistors of the static memory, that is connected to the self-emitting element that does not contribute to display is made a low voltage compared to the power supply for supplying current to the other transistor.

3. The active matrix display device of claim **1**, wherein:

a current control transistor separate from the transistors of the static memory is connected in series with the transistor connected to the self-emitting element that does not contribute to display, and current amount flowing in the self-emitting element that does not contribute to display is adjusted by adjusting the current amount of this current control transistor.

4. The active matrix display device of claim **1**, wherein:

a diode connected current control transistor separate from the transistors of the static memory is connected in series with the transistor connected to the self-emitting element that does not contribute to display, and current amount flowing in the self-emitting element that does not contribute to display is reduced.

5. The active matrix display device of claim **1**, wherein the self-emitting elements are organic EL elements.

* * * * *

专利名称(译)	有源矩阵显示装置		
公开(公告)号	US20100103181A1	公开(公告)日	2010-04-29
申请号	US12/531496	申请日	2008-03-12
[标]申请(专利权)人(译)	伊斯曼柯达公司		
申请(专利权)人(译)	伊士曼柯达公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	KAWABE KAZUYOSHI		
发明人	KAWABE, KAZUYOSHI		
IPC分类号	G09G3/32 G06T1/60 G09G5/00 G09G5/10		
CPC分类号	G09G3/3258 G09G2330/021 G09G2300/0857 G09G3/3291		
优先权	2007086530 2007-03-29 JP		
外部链接	Espacenet USPTO		

摘要(译)

该应用旨在减少在每个像素中具有静态存储单元的有源矩阵有机EL面板中不发光的像素的功耗。每个像素电路包括选择晶体管（5），第一（2）和第二（4）驱动晶体管以及分别连接到第一和第二驱动器的第一有机EL元件（1）和第二（3）有机EL元件晶体管。第二个有机。 EL元素被屏蔽，对像素亮度没有贡献。流过第二有机EL元件的电流通过限流装置减小。该电流限制装置可以是在与第二有机EL元件的电流路径中使用的第二电源电压（VDD2），第二电源电压低于与第一有机EL元件的电流路径的对应的第一电源电压（VDD1）。 。或者，电流限制装置可包括限流晶体管（11）或二极管连接的晶体管（13）。